EC

Notice of Allowability	Application No.	Applicant(s)	
	10/811,613	SOHN ET AL.	
	Examiner	Art Unit	
	Dang T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Applicant's arguments filed on 14 August 2006*.

2. ☒ The allowed claim(s) is/are *1,3-12,14-16 and 18-20*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Search history*.

Anh Phung

ANH PHUNG
PRIMARY EXAMINER

Response to Amendment

1. This office action is in response to applicant's arguments received on 8/14/06. Claims 1 – 3, 18 and 22 have been canceled. Claims 23 and 24 have been added. Claims 1, 3 – 12 and 14 – 16 and 18 - 20 are pending on this application. Claims 1 and 15 are independent claims.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Richard Ratchford on October 5, 2006.

The application has been amended as follows:

Amendment (for claim 1) A method of controlling an integrated circuit (IC) to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal and which comprises ~~a plurality of~~ memory blocks, each of the memory blocks comprising ~~a plurality of~~ sub-memory blocks, data memory blocks corresponding to the memory blocks, and a tag memory controlling unit, the method comprising:

(a) receiving a write address, a read address, and write data;

(b) determining, a in which sub-memory block of the sub-memory blocks and a in which data memory block of the data memory blocks ~~in which~~ a data read operation and a data write operation are to be performed in response to the write address and the read address by using the tag memory controlling unit;

(c) performing the data read operation or the data write operation in the data memory block according to the determination of step (b); and

(d) performing the data read operation or the data write operation in the sub-memory block according to the determination of step (b).

Cancel claim 2.

Amendment (for claim 3) The method of claim 1, wherein step (d) further comprises:

(d1) when the data read operation is performed, transmitting the read data to a transmitting unit corresponding to a the sub-memory block ~~inside the memory block~~;

(d2) transmitting the data ~~transmitted~~ to an output buffer; and

(d3) outputting the data transmitted to the output buffer.

Amendment (for claim 10) The method of claim 1, wherein if upper addresses of the received write address and read address are the same, the read address and the write address are not the same as a data memory address and data stored in the data memory block corresponding to the write address is valid, step (c) further comprises:

(c1) reading data stored in the data memory block corresponding to the write address; and

(c2) writing write data corresponding to the write address to the data memory block from which the data is read; and

step (d) further comprises:

(da) performing a data read operation in a sub-memory block corresponding to the read address; and

(db) writing the read data to a sub-memory block corresponding to the data memory block in which data read in step (c1) is stored.

Amendment (for claim 14) The method of claim 1, wherein the tag memory controlling unit writes data to the memory blocks or the data memory blocks or reads data from the memory blocks or the data memory blocks in response to the write address or the read address.

Amendment (for claim 15) A method for performing a write operation and a read operation in an integrated circuit (IC) comprising a separate input and output (I/O), ~~a plurality of~~ first memory locations ~~blocks~~, each of the first memory locations ~~blocks~~ comprising ~~a plurality of~~ third [[sub-]] memory locations ~~blocks~~, ~~data~~ second memory locations ~~blocks~~ corresponding to the first memory locations ~~blocks~~, and a memory controlling unit, the method comprising:

receiving a write address, a read address and a write data command during a period of a clock signal;

determining, a ~~first~~ third memory location of the third memory locations and a second memory location of the second memory locations, where a write operation

and a read operation are to be performed in response to the write address and the read address by using the memory controlling unit; and

performing the write operation in one of the ~~first~~ third memory location and the second memory location and the read operation in one of the ~~first~~ third memory location and the second memory location.

Cancel claim 17.

Amendment (for claim 18) The method of claim 15, wherein the determination step further comprises:

determining if the write address and the read address are input;

determining if an upper address of the write address is coincident with an upper address of the read address;

determining if the write address and the read address are coincident with a data memory address; and

determining if data stored in one of ~~the~~ a first memory location of the first memory locations and the second memory location is valid data.

Claim 20, line 3 changes "a third" To - - the third- -

Cancel claim 21.

Allowable Subject Matter

3. Claims 1, 3-12, 14–16, 18, and 18-20 are allowed.

4. The following is an examiner's statement of reasons for allowance:

With respect to claim 1, the prior art of record fails to anticipate or make obvious a method of controlling an integrated circuit (IC) to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal and which comprises memory blocks, each of the memory blocks comprising a sub-memory blocks, data memory blocks corresponding to the memory blocks, and a tag memory controlling unit, in combination with other limitations, the method comprising: "determining, in which sub-memory block of the sub-memory blocks and in which data memory block of the data memory blocks a data read operation and a data write operation are to be performed in response to the write address and the read address by using the tag memory controlling unit".

With respect to claim 15, the prior art of record fails to anticipate or make obvious a method for performing a write operation and a read operation in an integrated circuit (IC) comprising a separate input and output (I/O), first memory locations, each of the first memory locations comprising third memory locations, second memory locations corresponding to the first memory locations, and a memory controlling unit, in combination with other limitations, the method comprising: "determining, a third memory location of the third memory locations and a second memory location of the second memory locations, where a write operation and a read operation are to be performed in response to the write address and the read address by using the memory controlling unit".

Dependent claims 3 – 12, 14, 16, and 18 – 20 are allowed based on the allowance of the respective independent claims 1 and 15 above.

5. The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Hsiao et al., taken individually or in combination, do not teach the claimed invention of determining, in which sub-memory block of the sub-memory blocks and in which data memory block of the data memory blocks a data read operation and a data write operation are to be performed in response to the write address and the read address by using the tag memory controlling unit, in combination with other limitations.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

7. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703)

305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 10/12/2006

Anh Phung 10/16/06

ANH PHUNG
PRIMARY EXAMINER